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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/652,267
Filing Date: August 29, 2003
Appellant(s): ELZUR ET AL.

Ognyan Beremski
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed May 15, 2006 appealing from the Office action mailed October 7, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include: (1) a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters and (2) for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function as permitted by 35 U.S.C. 112, sixth paragraph, must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters. The brief is deficient because the summary only refers to the specification, and not to the drawings by reference characters.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,757,746	Boucher et al.	6-2004
6,427,173	Boucher et al.	7-2002
6,751,235	Susnow et al.	6-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-5 and 7-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Boucher et al. (USPN 6,757,746) (hereinafter Boucher).

1. Referring to claim 1, Boucher discloses a system for offloading TCP processing, the system comprising:

a host 100 (Figure 1);

a network interface card (i.e. network interface device 102) (Figure 1) coupled to said host (see parallel bus connecting 102 with 100), said NIC comprising:

a TCP enabled Ethernet controller (i.e. NIC including the ASIC 400 disclosed in Figure 21 of app. no. 09\464,283, USPN 6,427,173 incorporated by reference) comprising at least one internal elastic buffer (i.e. the transmit and receive sequencer 2104, 2105 Figure 21 of '173), wherein said TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming TCP packet in said internal elastic buffer, said processing occurring

without reassembly (i.e. the packet is DMA'd over to the host memory 110 and no reassembly done within the TEEC) (col. 5, lines 40-60).

2. Referring to claim 2, Boucher discloses said at least one internal elastic buffer comprises a receive internal elastic buffer 2105 and a transmit internal elastic buffer 2104 (Figure 21, col. 25, lines 1-15 of '173).

3. Referring to claims 3 and 4, Boucher discloses incoming TCP packets are temporarily buffered in said receive buffer and outgoing TCP packets are temporarily buffered in said transmit elastic buffer (col. 17, lines 35-67; col. 25, lines 1-15 of '173).

4. Referring to claim 5, Boucher discloses said TEEC places at least a portion of said incoming TCP packet data into at least a portion of a host memory (Boucher, Figure 2; col. 5, lines 50-55).

5. Referring to claim 7, Boucher discloses out of order tCP packets are not reordered in a TEEC buffer (i.e. they are reordered in the host memory) (Figure 2).

6. Referring to claim 8, Boucher discloses said NIC does not require a dedicated memory for reordering out of sequence TCP packets (i.e. the host memory is used) (Figure 2).

7. Claim 9 is rejected for similar reasons as stated above (i.e. it is inherent that any packet received would be inserted in its correct placement in host memory as shown by Figure 2).

8. Claims 10-13 are rejected for similar reasons as stated above (i.e. the Office takes the term "highest hierarchy" as the best place to put the information, and "single copy operation" as a DMA transfer).

9. Referring to claim 14, Boucher discloses the TEEC comprises a single chip having the buffer integrated therein (i.e. integrated into the Apollo VT8501 MVP4 Northridge chip) (col. 6, lines 15-25).

10. Claims 15-33 are rejected for similar reasons as stated above.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boucher.

11. Boucher discloses the invention substantively as described in claim 1. Boucher does not specifically state that only the elastic buffer is used to temporarily buffer at least a portion of the incoming TCP packet, however it is well known that elastic buffers are used to buffer packets (i.e. receiving FIFO's for routers, etc.). BY this rationale, "Official Notice" is taken that both the concept and advantages of providing for utilizing only the elastic buffer to temporarily buffer a portion of the TCP packet is well known

and expected in the art. It would have been obvious to one of ordinary skill in the art to modify the teaching of Boucher to include that only the elastic buffer is used to buffer the packet in order to utilize faster on chip memory rather than off-chip RAM, resulting in faster uploads to the host processor as well as reduced overhead regarding retrieving information from off chip memory.

(10) Response to Argument

Appellant's arguments have been fully considered but are not persuasive.

In the remarks (Brief, pages 7-29), Appellant argues, in substance, that (A) Boucher does not teach processing occurring without reassembly (Brief, page 8), (B) Boucher does not teach "a TEEC including at least one internal elastic buffer, wherein the TEEC processes an incoming TCP packet once and temporarily buffers at least a portion of said incoming packet in said internal elastic buffer (Brief, page 13) (C) Boucher does not disclose at least one internal elastic buffer is one of a receive elastic buffer and a transmit elastic buffer (Brief, page 16), (D) Boucher does not disclose a portion of the incoming TCP packet is temporarily buffered in the receive elastic buffer and transmit internal elastic buffer (Brief, page 17), (E) Boucher does not disclose the TEEC places a portion of the TCP packet into a host memory (Brief, page 18), (F)Boucher does not disclose out of order TCP packets are not at least one of stored, re-ordered and reassembled in a TEEC buffer (Brief, pages 18-19), (G) Boucher does

not disclose said NIC does not require a dedicated memory for re-ordering out-of-sequence TCP packets (Brief, page 19), (H) Boucher does not disclose the TEEC places data from the TCP packet into a highest hierarchy of buffer available in a host memory by performing a single copy operation (Brief, page 20), (I) Boucher does not disclose the TEEC comprises a single chip, having integrated therein, at least one internal elastic buffer (Brief, page 21), (II) Appellant argues the inherency of claim 9, stating that it is not necessarily true that any packet received would be automatically placed in the correct placement, (III) Susnow does not disclose or suggest that data is temporarily stored only by the elastic buffer (Brief, page 27).

As to point (A), once again Appellant is attempting to redefine the term "reassembly" as something completely different than what the invention actually does. The Examiner has clearly shown that the specification teaches (page 11, ¶ 39) that reassembly is dealing with reassembling TCP/IP packets which were fragmented. Although limitations are not imported into the claims, Appellant is bound by the specification as to what is actually disclosed. If Appellant is attempting to mean "reassembly" as any other meaning, then a rejection under 35 USC 112, first paragraph is necessitated, since Appellant does not enable this meaning of the term "reassembly". Furthermore a rejection under 35 USC 112, second paragraph is also warranted as being an indefinite negative limitation because it is an attempt to claim the invention by excluding what the inventors did not invent rather than distinctly and particularly pointing out what they did invent. In re Schechter, 205 F.2d 185, 98 USPQ 144 (CCPA 1953).

Also see MPEP 2173.05(i). Furthermore Appellant attempts to state that the receive sequencer 2105 and data assembly register 2202 *clearly* show that the register is used to assemble data. Appellant should be aware that "assembling" data and "reassembling" data is not the same. Reassembling data, as limited by the specification, deals only with reassembling fragmented packets (see cited portions of the specification above). The packets are "assembled" in the NIC card of Boucher by clocking in specific bits of data in order to correctly route/forward the packet (See Boucher '173, col. 27, lines 12-15, the register is a "shift register 2217" wherein data is loaded serially a single byte at a time and is unloaded in parallel). This is what Appellant is attempting to equate to the claimed "processing without reassembly". Appellant does not enable this, does not disclose this, and therefore cannot utilize this definition of the term "reassembly" as an attempt to state Boucher does not meet the claimed invention. By this rationale, the rejection should be maintained.

As to point (B) Appellant has not sufficiently defined what is meant by an "elastic buffer". The Examiner equates the claimed "elastic buffer" to the data synchronization buffer 2200 on the ASIC chip as found in Boucher '173 (Figure 21 shows the ASIC 400 encompasses the receiving sequencer 2105; as shown in Figure 22, the data sync buffer 220 is clearly within the receiving sequencer 2105 and is therefore on the ASIC 400). The Office has interpreted the term "elastic buffer" with the scope commensurate with the specification and has construed the term as "not a multi-megabyte memory that

is utilized for packet reordering reassembly or retransmission" (as used in the specification, page 11, ¶ 39). By this rationale, the rejection should be maintained.

As to points (C) and (D), the data sync buffer stores packets as they are being received. Any packet received is transmitted to the host memory to be reassembled, and therefore can be construed as the transmit internal elastic buffer as well. Therefore the data sync register can be both the receiving and transmitting internal elastic buffer. The claimed invention does not state multiple elastic buffers. By this rationale, the rejection should be maintained.

As to point (E), Appellant is incorrect. Appellant's attention is directed to Figure 2 of Boucher where it shows that the packets 200 on NI device 102 are transmitted to the Host 100 memory. By this rationale, the rejection should be maintained.

As to point (F), Appellant is incorrect. In conjunction with (E) above, it can be clearly shown that the multi-packet message 200 in Figure 2 is reassembled in the Host memory 110. By this rationale, the rejection should be maintained.

As to point (G), since the NIC device does not do any reordering, the NIC card does not require dedicated memory to conduct such reordering. The data is automatically DMA'd over to the host memory.

As to point (H), Appellant has not sufficiently meant what is meant as to the "highest hierarchy" in the claim and as such the Examiner has interpreted this commensurate with the scope of the claim. As such the Examiner has construed this phrase as as the best place to put the information, and "single copy operation" as a DMA transfer. Appellant has not attempted to redefine or explain what is meant by either of these terms and as such these terms have been interpreted by the Examiner. By this rationale, the rejection should be maintained.

As to point (I), Appellant is incorrect, see response to point (B) above where it is clearly shown that the data sync buffer is within the ASIC. By this rationale, the rejection should be maintained.

As to point (II), the host memory is used to assemble packets fragmented at the IP layer (see Figure 2, the multi-packet memory 200 is reassembled in the host memory). The features of Figure 2, clearly indicate that when a multi-packet message is received by the NI device, that the data would be inserted into the host memory. By this rationale, the rejection should be maintained.

As to point (III), Appellant is incorrect. A thorough examination of Susnow clearly shows that the elastic buffer of Susnow (Figure 8, ref. 682, the entire figure is the only memory element used to buffer data between different networks without underflow or overflow. The elastic buffer is the *only* buffer used in Susnow to temporarily buffer data.

Furthermore since the data is used *temporarily*, it can be construed that there is a time period associated with the storage of data in the elastic buffer. Therefore other memory elements can store the data either before or after the elastic buffer stores the data. By this rationale, the rejection should be maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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